BEE 271 Digital circuits and systems
Spring 2017
Lab 1: Digital logic devices instructor's notes*

4 Boolean functions

4.1 7400 NAND gate

Build the circuit in figure 8 with red LEDs and 470 Ω resistors. Lit LED = 1, not lit = 0. Construct a truth table.

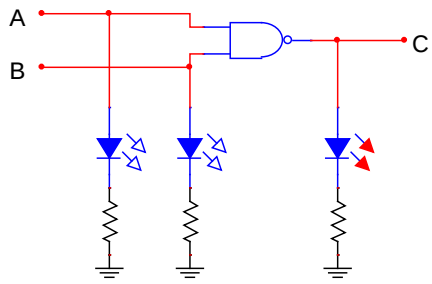


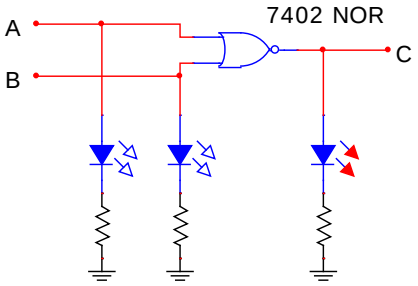
Figure 8. Testing NAND gate Boolean functions.

Here is the expected result.

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

4.2 7402 NOR gate

Rewire your circuit with a 7402 NOR gate in place of the NAND and construct a truth table.

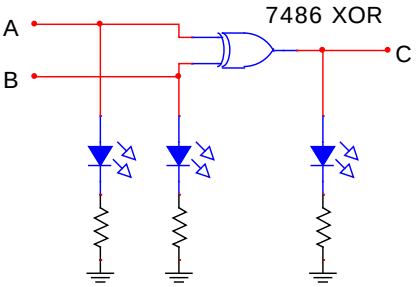


Here is the expected result.

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

4.3 7486 XOR gate

Rewire your circuit with a 7486 XOR gate in place of the NOR and construct a truth table.



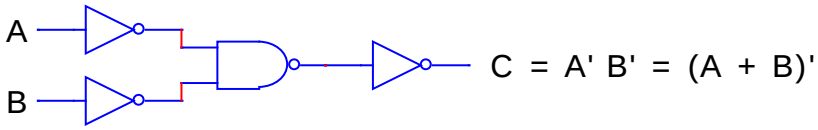
Here is the expected result.

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

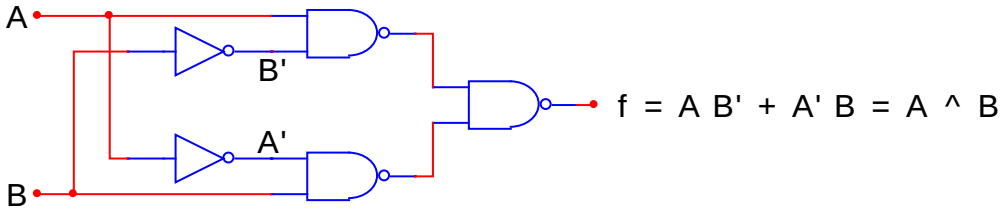
* These notes were written by Nicole Hamilton.

4.4 Analysis

1. Design a NOR function using one NAND gate and three inverters.



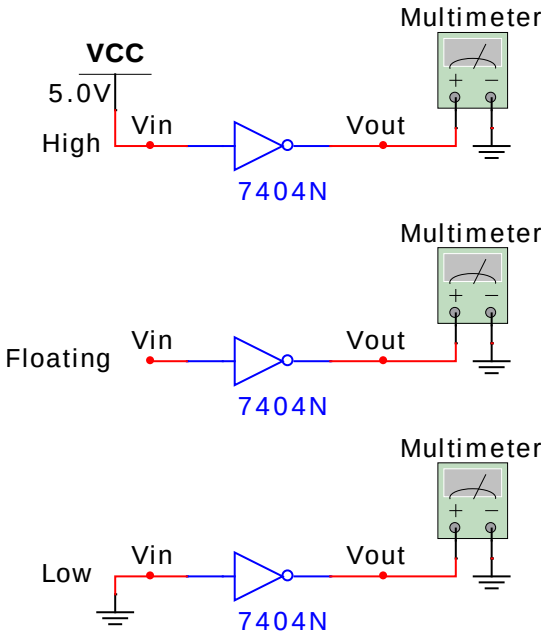
2. Design an XOR function using no more than three NAND gates and two inverters.



3. If a square wave is fed into one input to an XOR gate and the other input is tied high, will the output be the same as the input square wave or will it be inverted? What if the other input is tied low?

   It'll be the same if the other input is tied low and inverted if it's tied high.

5 Device characterization



5.1 TTL logic levels

Construct a table of measurements of Vout for a 7404 inverter with the input tied high, left floating and tied low as shown in figure 10.

Figure 10. Measuring Vout with the input tied high, left floating (not connected) or tied low to ground (0 V).

Here are some typical results with an LS part. A floating input looks like a 1.

Input	Output	Logic level
High	120 mV	0
Floating	120 mV	0
Low	4.43 V	1

5.2 Switching thresholds

Using the function generator to drive the inverter as in figure 11, set Vin = 5.0 Vpp +2.5 V offset 1 KHz triangle wave and check your setting on the oscilloscope.

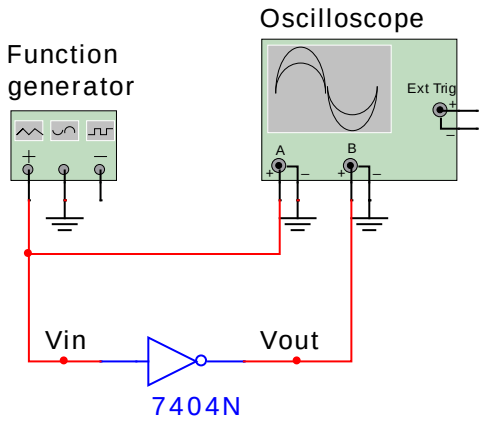
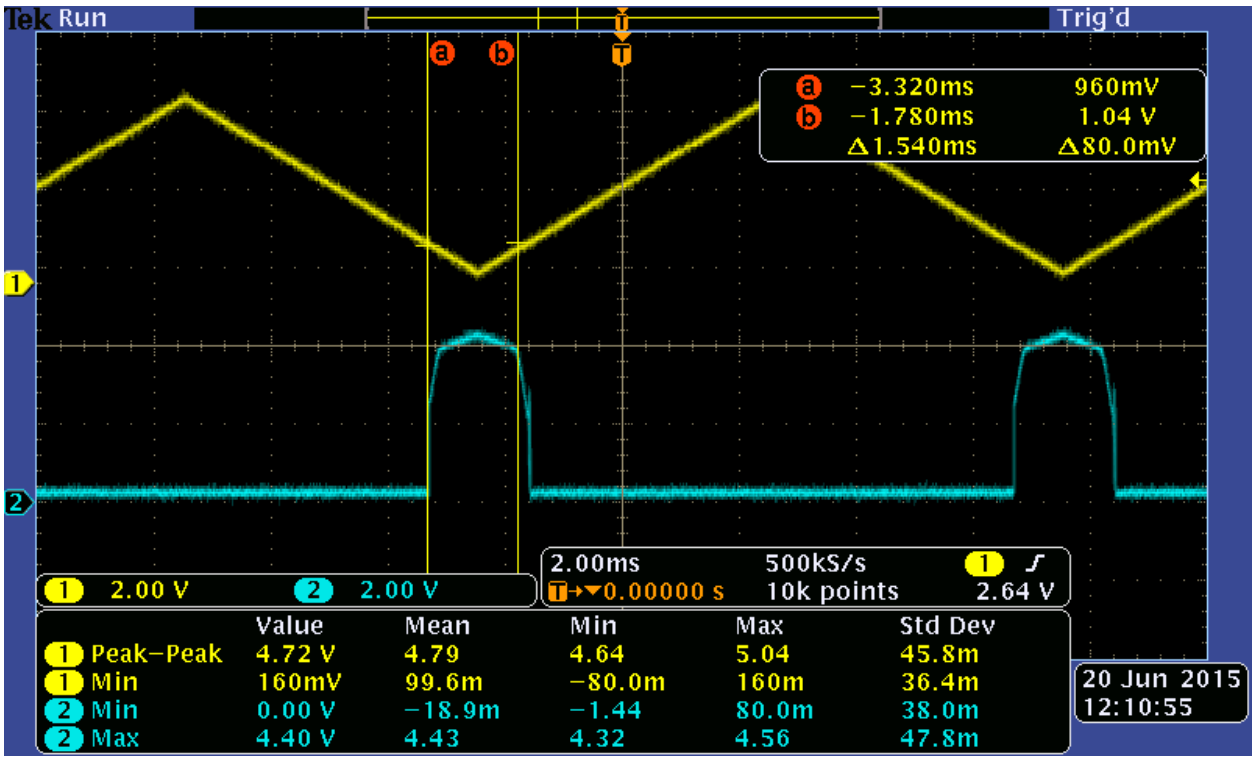


Figure 11. Measuring switching thresholds and transient response under no-load conditions.

Capture a screenshot similar of Vin and Vout with cursors positioned to measure Vin at the points where Vout begins to change and on-screen measurements Vin peak-to-peak and Vout min and max.

Here is a typical result with a standard part. Note the function generator has been set properly to 5.0 Vpp +2.5 V offset. Cursors are on input and positioned where Vout just begins to switch, at Vin = 960 mV falling or 1.04 V rising.

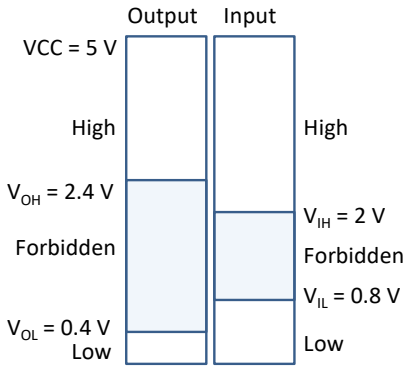

Tek Run
Trig'd
a −3.320ms 960mV
b −1.780ms 1.04 V
Δ1.540ms Δ80.0mV
1 2.00 V
2 2.00 V
2.00ms 500kS/s
0.00000 s 10k points
2.64 V
Value Mean Min Max Std Dev
1 Peak−Peak 4.72 V 4.79 4.64 5.04 45.8m
1 Min 160mV 99.6m −80.0m 160m 36.4m
2 Min 0.00 V −18.9m −1.44 80.0m 38.0m
2 Max 4.40 V 4.43 4.32 4.56 47.8m
20 Jun 2015
12:10:55

5.3 Analysis

1. Compare your measured values for high and low output levels with the input switching threshold measured with the ramp. How much margin did you find between the high and low output levels and input threshold switching level?

   Here are some typical results. Notice the actual margins are typically much larger than the minimum 0.4 V guaranteed by the TTL standard.

Logic value	Measured output level	Measured switching threshold	Margin
0	120 mV	960 mV	840 mV
1	4.43 V	1.04 mV	3.39 V



2. When driven by a triangle, was the output a symmetric square wave with a 50% duty cycle? Why or why not?

   This question asks if the output was truly a square wave with equal amounts of time spent as a 1 and as a 0.

   The duty cycle depends on your device and where it switches but it will certainly not be 50%. The midpoint of the triangle input was 2.5 V but the TTL switching levels are centered around 1.4 V.

   My own sample gate interpreted anything over about 1.0 V as a logic 1, which was a lot more than half the time, causing the output to be a 0 more than 50% of the time.

5.4 Transient response

Using the function generator to drive the inverter, again as in figure 11, set Vin = 5.0 Vpp +2.5 V offset 1 KHz square wave and check your setting on the oscilloscope.

Capture screenshots on the oscilloscope of Vin on channel 1 and Vout on channel 2 with appropriate cursors and on-screen measurements of the following characteristics as shown in figures 12 and 13.

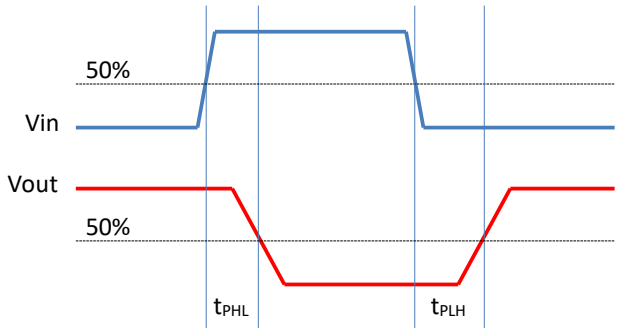


Figure 12. t_{PHL} and t_{PLH} are measured from input to output.

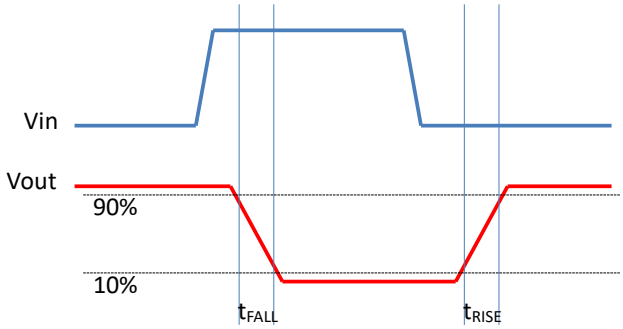
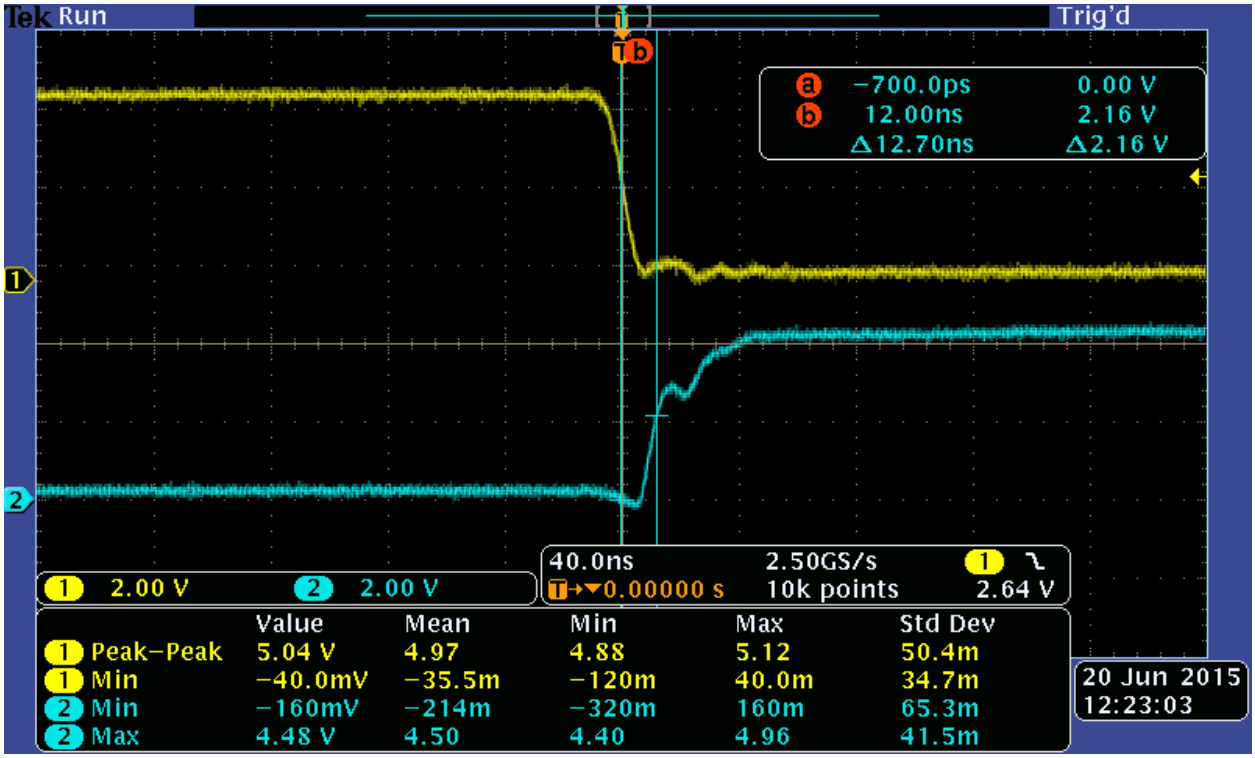


Figure 13. t_{FALL} and t_{RISE} are measured on the output only.

1. t_{PLH}, the propagation time from the 50% point on the input to the 50% point on the output for a low-to-high output transition.

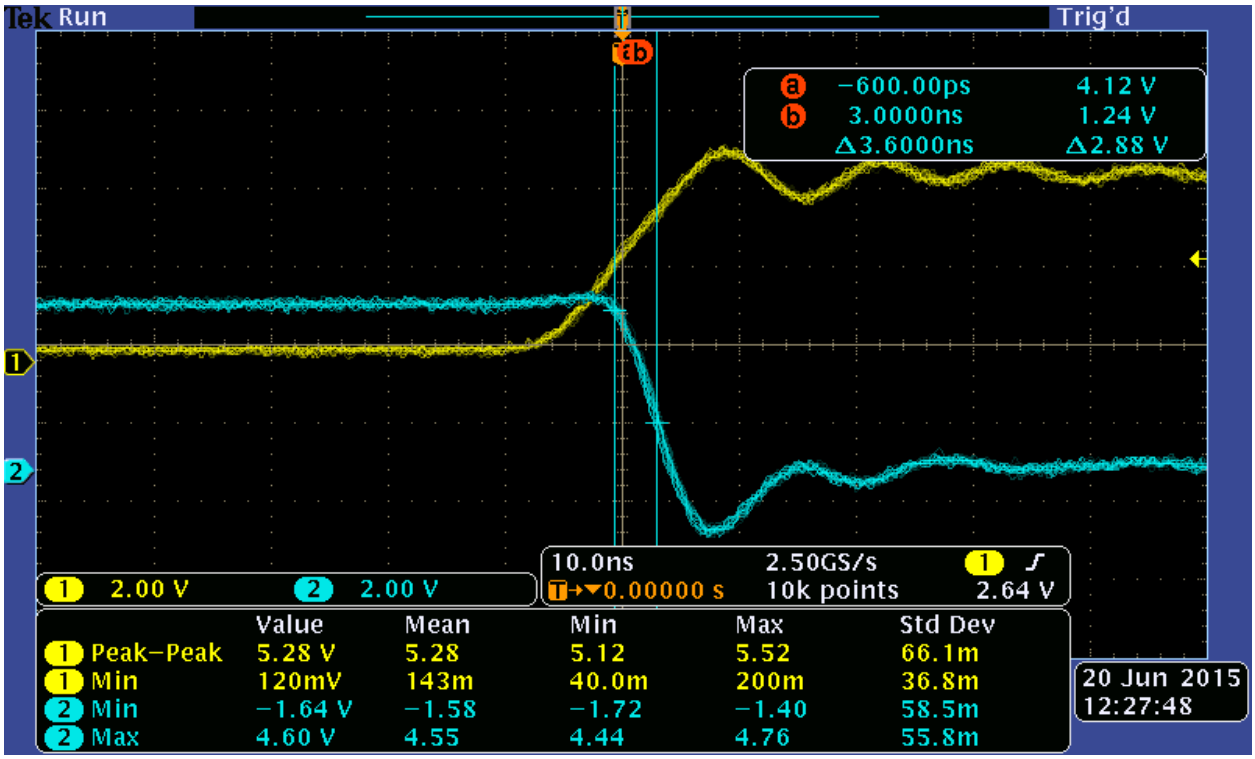
   Here is a typical screenshot. Note the cursors and on-screen measurements.

   For this gate, a standard 7400xx part, t_{PLH} = 12.7 ns.



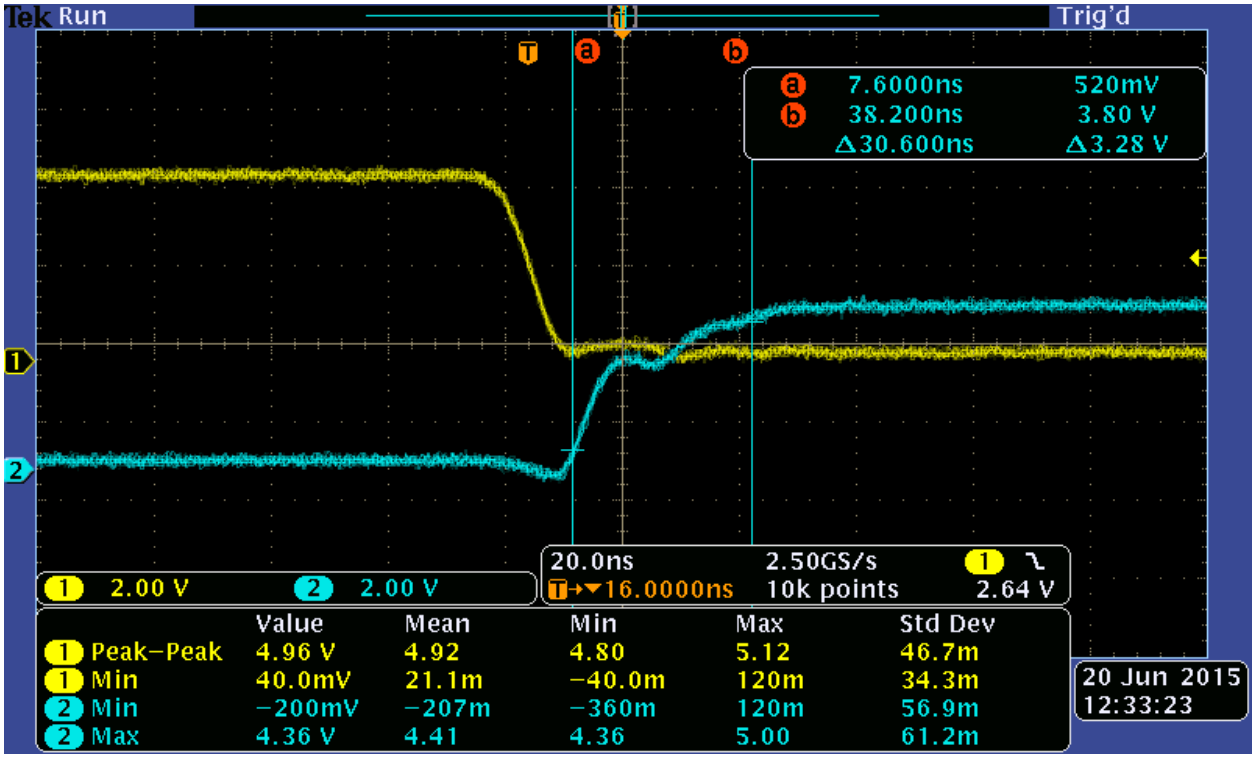
2. t_{PHL}, the propagation time from the 50% point on the input to the 50% point on the output for a high-to-low output transition.

   Here is a typical screenshot. Note the cursors and on-screen measurements. For this gate, a standard 7400xx part, t_{PHL} = 3.6 ns. (The output falls a lot faster than it rises.)



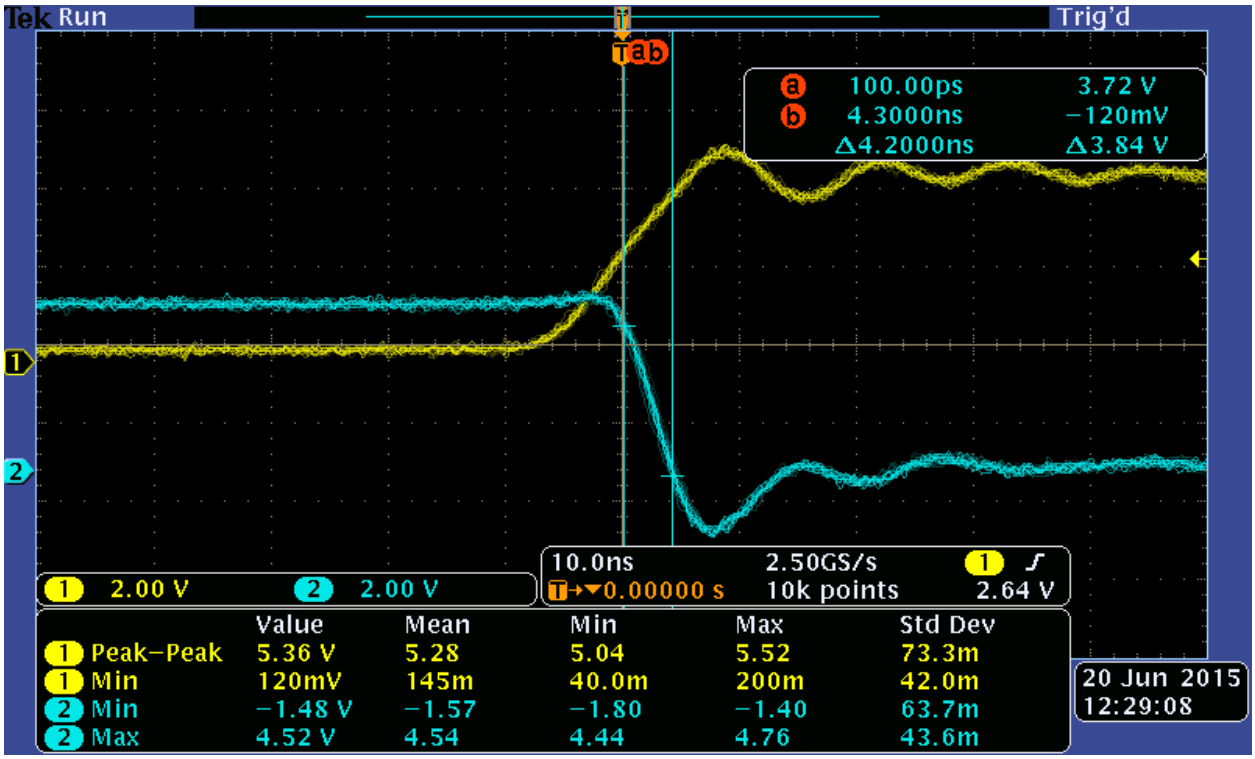
3. t_{RISE}, the time for the output to go from 10% to 90% rising.

   Here is a typical screenshot. Note the cursors and on-screen measurements.
   For this gate, a standard 7400xx part, t_{RISE} = 30.6 ns.



4. t_{FALL}, the time for the output to go from 90% to 10% falling.

   Here is a typical screenshot. Note the cursors and on-screen measurements. For this gate, a standard 7400xx part, t_{FALL} = 4.2 ns. (Again, it's much faster falling.)



5.5 Analysis

1. Is a TTL device equally fast switching from high-to-low and low-to-high?

   It depends on your device. With a standard 74xx part like mine, it's a lot faster switching high-to-low than low to high. With a 74LSxx part, the switching times may be a lot closer.

	Propagation (ns)	Rise/fall (ns)
Low-to-high	12.7	30.6
High-to-low	3.6	4.2

6 Active low versus active high

Build the two circuits shown in figure 14 side-by-side using two NAND gates and two 470 Ω resistors. Both LEDs should light up. Record the measured values of your resistors, the power supply voltage and the voltages at A and B.

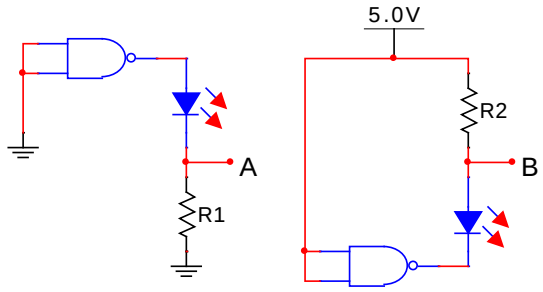


Figure 14. Active high on the left, active low on the right.

The circuit on the left is called active high because the LED turns on (activates) when the output from the NAND is high = 1. The one on the right is called active low because the LED turns on when the output is low = 0.

Typical approximate measured values with an LS part:

VCC = 5.0 V
R1 and R2 = 470 Ω
VA = 2.84 V
VB = 2.16 V

6.1 Analysis

1. Is the LED brighter in the active low or the active high circuit?

   Depends on the type of TTL chip you got in your kit. If it's a standard SN74xx part, it's usually brighter in active low because in the high state, the output is only about 4.5 V. If you have a low power Shottky SN74LSxx part, you probably won't see much difference at all.

2. Calculate the voltage across each resistor, VR1 = VA and VR2 = 5.0 – VB. Using Ohm's Law, I = V / R, calculate the current through each resistor and thus, through each the diode when it's on in the active high and active low configurations.

   With an LS part, there might not be any difference.
   VR1 = VA = 2.84 V
   VR2 = 5.0 – 2.16 = 2.84 V
   IR1 = VR1 / R1 = 2.84 / 470 = 6.04 mA
   IR2 = VR2 / R2 = 2.84 / 470 = 6.04 mA

7 Ring oscillator

7.1 Circuit

Build the circuit in figure 15 using five inverters.

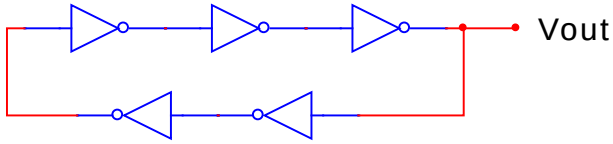
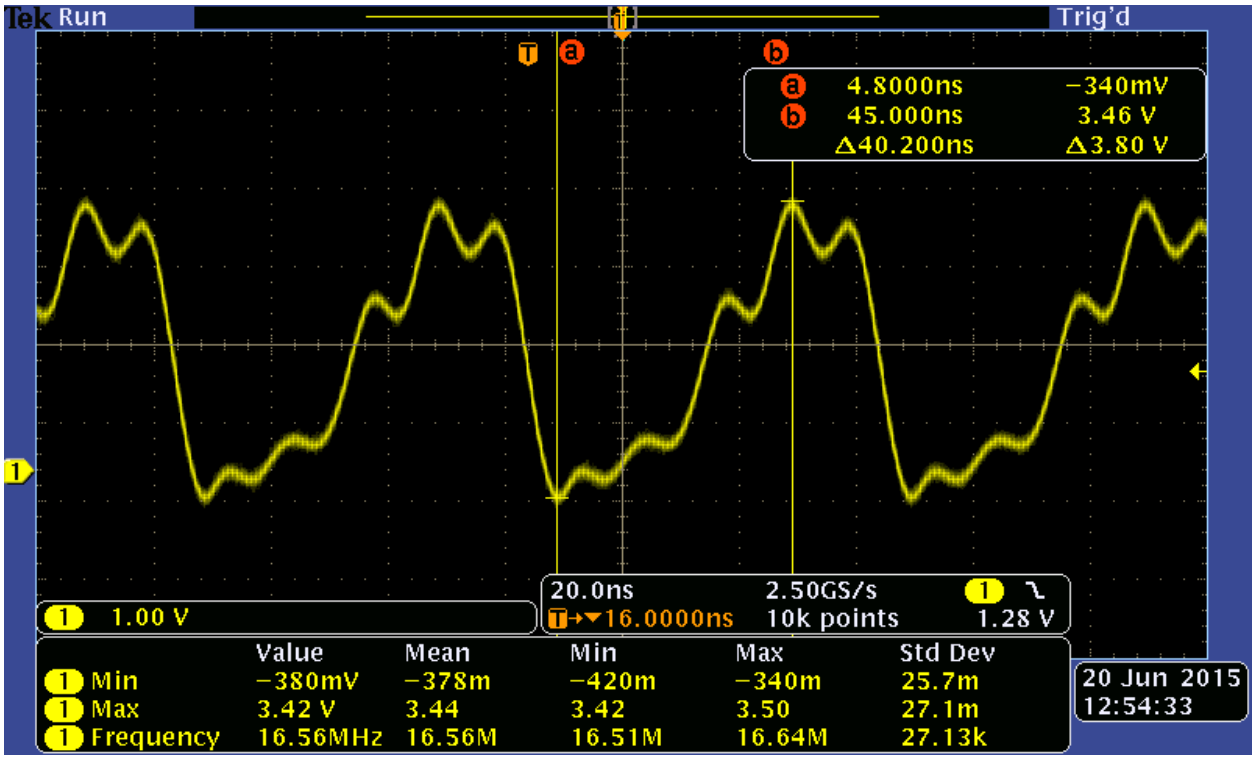


Figure 15. A ring oscillator.

7.2 Measurements

Capture screenshots of the output with on-screen measurements of frequency and peak-to-peak voltage.

Here is a typical result.



7.3 Analysis

1. Explain how this circuit works.

   Whatever the state at any given node, whether a 0 or a 1, if it's fed through 5 inverters, it comes back inverted, flipping the node to the new state.

2. What is the relationship between the output frequency and the rise and fall times you measured for an inverter?

   The period is related to the propagation and rise and fall times around the ring: We need 5 low-to-high + 5 high-to-low transitions for a complete cycle. The allows us to crudely estimate the expected period, T, and frequency, f, as follows.

   T = 5 (tPLH + tPHL) = 5 (12.7 + 3.6) = 81.5 ns
   f = 1 / T = 12.3 MHz

   This agrees reasonably well with the measured result of 16.6 MHz.

   The shape, especially all the wiggling, is because when a gate switches, there's always a lot of ringing in the output before it settles. In this circuit, we have 5 of them doing that as fast as they can. That produces a lot of noise on the power supply and likely explains a lot of it.

8 Latch

Build the circuit in figure 16 using two NAND gates, two 10K resistors, two LEDs and two 470 Ω resistors. Alternate briefly shorting the S* input to ground, then briefly shorting the R* input to ground. Repeat this several times until you discover what this circuit does.

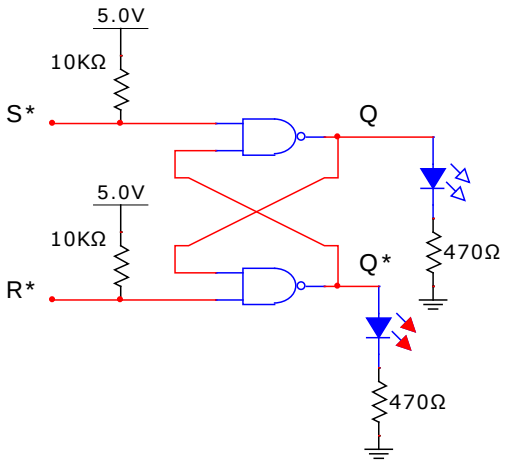


Figure 16. Latch.

8.1 Analysis

1. What does the latch do and how does it work?

   This circuit remembers its state when both S* and R* are left high = 1. It "latches" data. Q is the bit of data it remembers.

2. What do the S* and R* inputs do?

   If S* is pulled low = 0, Q goes to 1. S* is the (set)' input. If R* is pulled low = 0, Q* goes to 1. R* is the (reset)' input. We can summarize this as a truth table.

S*	R*	Q	Q*
0	0	1	1
0	1	1	0
1	0	0	1
1	1	Previous state	

9 Hazards

Build the circuit in figure 17.

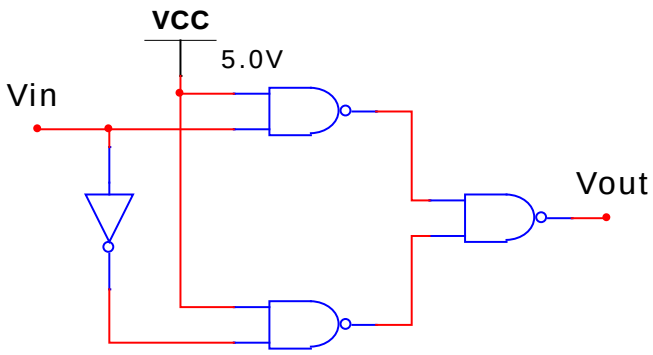


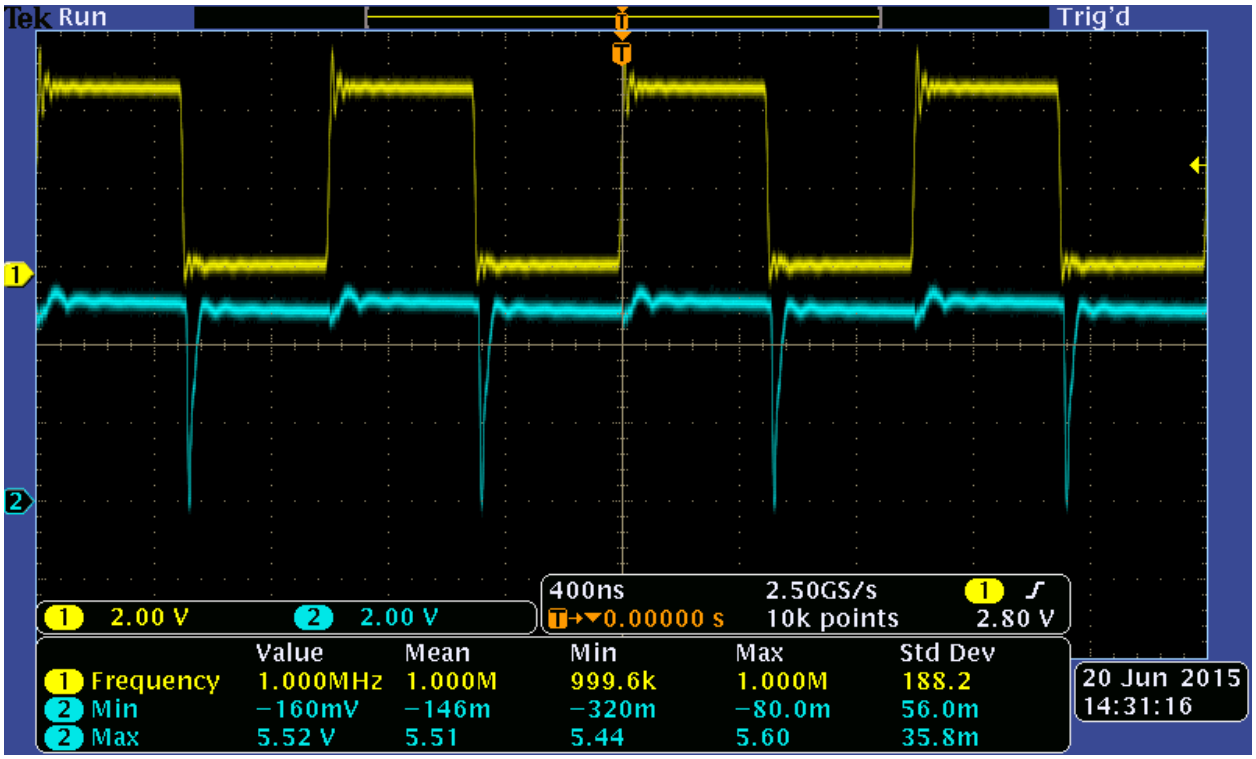
Figure 17. A circuit with a hazard.

9.1 Measurement

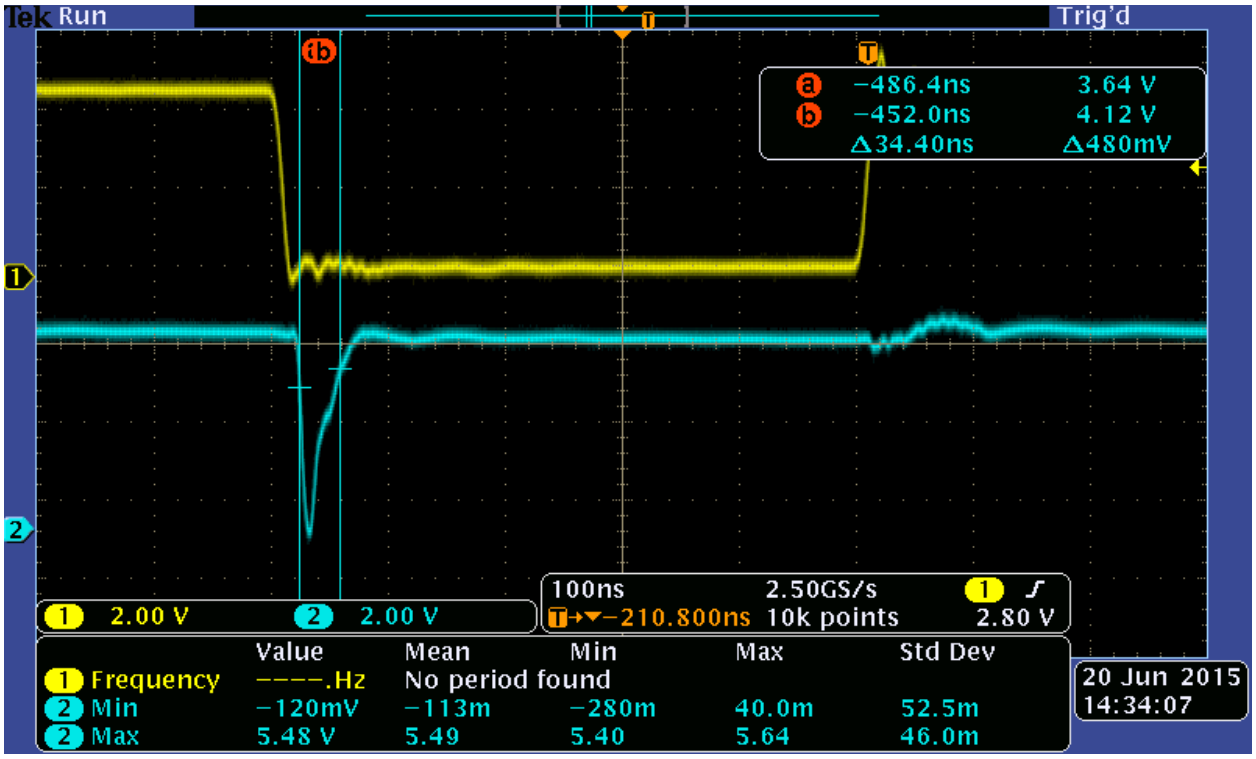
Set Vin = 5.0 Vpp +2.5 V offset 1 MHz square wave.

Capture screenshots of Vin and Vout with suitable cursors and on-screen measurements showing how the circuit behaves when Vin transitions low-to-high and high-to-low.

Here is a typical result showing that when the input transitions from 1 to 0, the output briefly blips to 0. On input transitions from 1 to 0, the output wiggles a little, but it stays a 1.



Zooming in:



9.2 Analysis

1. What is the expected output for Vin high? For Vin low? When Vin changes from 1 to 0 or from 0 to 1, should Vout change?

   Regardless of whether Vin = 0 or Vin = 1, we expect Vout should be 1.

2. What do observe?

   It blips to a 0 when the input transitions from high-to-low.

3. Explain what you observed.

   There's a delay through the inverter. When the input switches from 1 to 0, the 0 reaches the NAND gate at the top immediately. But there's a delay before the output of the inverter switches from 0 to 1. So there's a brief period when both NANDs see a 0 on one input, causing the outputs of both to be equal to 1. If both inputs to the final NAND = 1, the output is 0 (briefly).

4. Why do you think this is called a hazard?

   Because you just don't expect it.